WHAT IS CLAIMED IS:

1. 1. A trench transistor comprising:

a substrate having a surface;

a trench extending a selected depth into the substrate from the surface, the trench having a sidewall;

a gate structure at least partially within the trench; and

a source region self-aligned to the gate.

2. The trench transistor of claim 1 wherein the source region overlaps a portion of the gate structure.

3. The trench transistor of claim 2 wherein a gate-to-source capacitance arises from the overlap between the gate structure and the source region, the gate-to-source capacitance being selected according to the overlap.

4. The trench transistor of claim 1 wherein the source region forms a p-n junction in the substrate at a selected distance from the sidewall, the p-n junction, at least a portion of the p-n junction being essentially parallel to the sidewall.

5. The trench transistor of claim 1 further comprising a source contact region, the source contact region extending a selected distance into the substrate from the surface, wherein the source contact region forms an inner corner with the source region.

6. The trench transistor of claim 5 wherein the distance of the source p-n junction from the sidewall is essentially equal to the distance of the extension of the source contact region from the surface.

7. The trench transistor of claim 5 wherein both the distance of the source p-n junction from the sidewall and the distance of the extension of the source contact region from the surface is less than or equal to about 0.15 microns.

8. The trench transistor of claim 1 wherein the gate structure is recessed from the surface.

9. The trench transistor of claim 6 further comprising a heavy body, the heavy body extending into the inner corner formed by the source region and the source contact region.

10. A trench transistor comprising:

a substrate having a surface;

a trench extending a selected distance into the substrate from the surface, the trench having a sidewall;

a gate structure at least partially within the trench, the gate structure being recessed from the surface;

a source region self-aligned to the gate structure, the source region overlapping a portion of the gate structure and forming a p-n junction at a selected distance of less than or equal to about 0.15 microns from the sidewall, at least a portion of the p-n junction being parallel to the sidewall;

a source contact region extending less than or equal to about 0.15 microns from the surface, the source contact region forming an inner corner with the source region; and

a heavy body extending into the inner corner.

11. A method of forming a source region in a trench transistor, the method comprising:

a) forming a trench in a substrate, the substrate having a surface and the trench having a sidewall;

b) forming a gate structure in the trench; and

c) implanting source dopant such that at least a portion of the source dopant is implanted through the sidewall.

12. The method of claim 11 wherein a further portion of the source dopant is implanted opposite a portion of the gate structure.

13. The method of claim 11 further comprising, after the step (c),

d) implanting source dopant such that a second portion of the source dopant is implanted through a second sidewall of the trench.

WHAT IS CLAIMED IS:

1. 1. A trench transistor comprising:

a substrate having a surface;

a trench extending a selected depth into the substrate from the surface, the trench having a sidewall;

a gate structure at least partially within the trench; and

~~a source region self-aligned to the gate.~~

2. The trench transistor of claim 1 wherein the source region overlaps a portion of the gate structure.

3. The trench transistor of claim 2 wherein a gate-to-source capacitance arises from the overlap between the gate structure and the source region, the gate-to-source capacitance being selected according to the overlap.

4. The trench transistor of claim 1 wherein the source region forms a p-n junction in the substrate at a selected distance from the sidewall, the p-n junction, at least a portion of the p-n junction being essentially parallel to the sidewall.

5. The trench transistor of claim 1 further comprising a source contact region, the source contact region extending a selected distance into the substrate from the surface, wherein the source contact region forms an inner corner with the source region.

6. The trench transistor of claim 5 wherein the distance of the source p-n junction from the sidewall is essentially equal to the distance of the extension of the source contact region from the surface.

7. The trench transistor of claim 5 wherein both the distance of the source p-n junction from the sidewall and the distance of the extension of the source contact region from the surface is less than or equal to about 0.15 microns.

5 ~~8.~~ The trench transistor of claim 1 wherein the gate structure is recessed from the surface.

9. The trench transistor of claim 6 further comprising a heavy body, the heavy body extending into the inner corner formed by the source region and the source contact region.

7 ~~10.~~ A trench transistor comprising:

a substrate having a surface;

a trench extending a selected distance into the substrate from the surface, the trench having a sidewall;

a gate structure at least partially within the trench, the gate structure being recessed from the surface;

a source region self-aligned to the gate structure, the source region overlapping a portion of the gate structure and forming a p-n junction at a selected distance of less than or equal to about 0.15 microns from the sidewall, at least a portion of the p-n junction being parallel to the sidewall;

a source contact region extending less than or equal to about 0.15 microns from the surface, the source contact region forming an inner corner with the source region; and

a heavy body extending into the inner corner.

11. A method of forming a source region in a trench transistor, the method comprising:

a) forming a trench in a substrate, the substrate having a surface and the trench having a sidewall;

b) forming a gate structure in the trench; and

c) implanting source dopant such that at least a portion of the source dopant is implanted through the sidewall.

12. The method of claim 11 wherein a further portion of the source dopant is implanted opposite a portion of the gate structure.

13. The method of claim 11 further comprising, after the step (c),

d) implanting source dopant such that a second portion of the source dopant is implanted through a second sidewall of the trench.

14. The method of claim 13 further comprising, between the steps (c) and (d), rotating the substrate 180 degrees about an axis of implantation.

15. The method of claim 11 wherein the source dopant is arsenic.

16. A method of forming a source region in a trench transistor, the method comprising:

a) forming a trench in a substrate, the substrate having a surface and the trench having a first sidewall and a second sidewall;

b) forming a gate structure in the trench;

c) implanting a first dose of arsenic such that a portion of the first dose is implanted through the first sidewall, and a further portion of the first dose is implanted through the surface;

d) rotating the substrate 180 degrees about an axis of implantation; and

e) implanting a second dose of arsenic such that a portion of the second dose is implanted through the second sidewall, and a further portion of the second dose is implanted through the surface.

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